Quantum Computing for Earth Observation

Machines Roadmap Assessment Report (WP3)

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1 Scope of the document and terminology

This study provides a comprehensive overview of existing QC technologies and assesses their maturity. For each identified QC technology, we studied the current state of development, assessed the risks and estimated their future evolution. Based on these assessments, we provide our judgement on current and future readiness level of these platforms as well as their applicability to different applications. We employ information, material and publications which are publicly available, combined with the expert assessment of the WP team.

1.1 Applicable Documents

[AD-1]   QC4EO Study Statement of Work
[AD-2]   Proposal submitted for QC4EO
[WP2-del]   Deliverable of WP2

1.2 Acronyms

CMOS   Complementary Metal-Oxide-Semiconductor
FTQC   Fault-Tolerant Quantum Computing
GBS   Gaussian Boson Sampling
GKP   Gottesman-Kitaev-Preskill
HHL   Harrow-Hassidim-Lloyd
ML   Machine Learning
MZM   Majorana Zero Modes
NISQ   Noisy Intermediate-Scale Quantum
NP   Non-deterministic Polynomial
NV   Nitrogen Vacancy
QAOA   Quantum Approximate Optimization Algorithm
QC   Quantum Computing
QC4EO   Quantum Computing For Earth Observation
QEC   Quantum Error Correction
QFS   Quantum Flagship
QFT   Quantum Fourier Transform
QML   Quantum Machine Learning
QNN   Quantum Neural Network
QPU   Quantum Processing Unit
QTRL   Quantum Technology Readiness Level
QUBO   Quadratic Unconstrained Binary Optimization
TRL   Technology Readiness Level

2 Introduction and Overview of Quantum Computing Hardware Platforms

Qubits are the fundamental building blocks of quantum information processing. Qubits refer to quantum systems with two basis states (commonly labelled as $|0\rangle$ as $|1\rangle$). There are many different objects in Nature which may realize a qubit. However, to build a quantum computer, one needs "well-behaved" qubits and the ability to control them. Overall, there exist several criteria for a physical system to be able to act as a quantum computer, known as the DiVincenzo's criteria. Those are

1. A scalable physical system with well-characterized qubit.

2. The ability to initialize the state of the qubits to a simple fiducial state.

3. Long relevant decoherence times.

4. A "universal" set of quantum gates.

5. A qubit-specific measurement capability.

Various technologies (hereafter referred to as "quantum computing platforms") satisfy these criteria to various degree. These include superconducting circuits, trapped ions, photons, cold atoms, solid-state spins and more. In order to asses vendor roadmaps accurately it is useful to summarize the main technologies for realizing qubits. As we are interested in long-term prognosis (10+ years) as well as NISQ technologies (3-5 years), we also mention technologies that are currently relatively underdeveloped (topological qubits).

2.1 Superconducting Qubits

A superconducting qubit stores its quantum information in a miniature superconducting circuit. There are three categories of superconducting qubits: charge qubits, flux qubits and phase qubits. Charge qubits store information in the number of excess electrons on a capacitor, while flux qubits store information in the magnetic flux through a superconducting loop. Phase qubits use the phase difference between two superconducting states to store information.
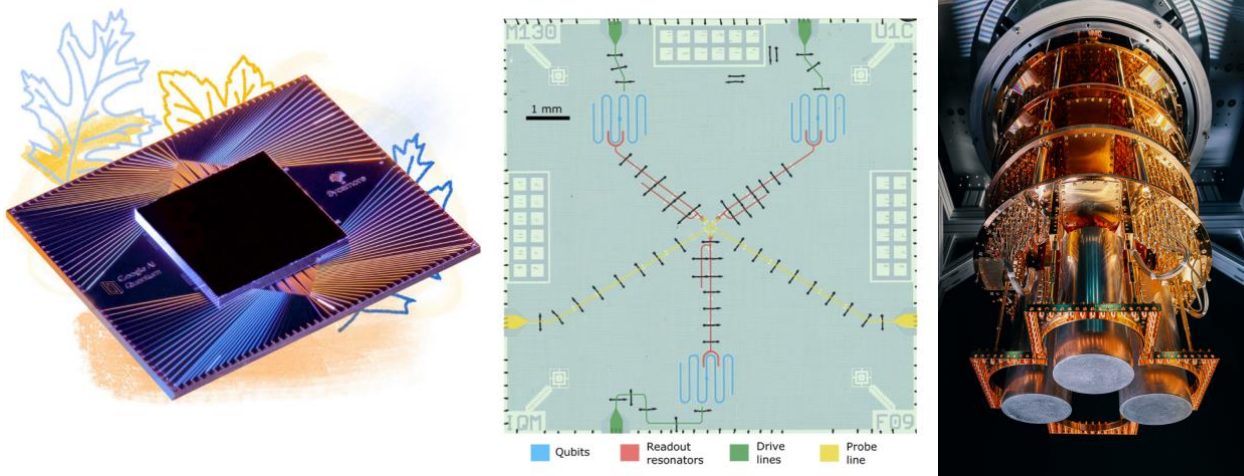
*Figure 1: Superconducting Quantum Computers. (**Left**) QPU chip . (**Middle**) layout of an IQM test chip. (**Right**) Wiring of a superconducting QPU in a cryostat.*

Superconducting qubits together with their operational components (drive lines, probe lines, readout resonators) are placed on a chip which is then cooled to very low temperatures to trigger the superconductivity and reduce the noise levels (typically around 10 mK). Once the qubit is cooled, it can be manipulated by applying microwave pulses to the circuit via the drive lines / resonators.

Superconducting qubits offer high degree of control and very fast gate times. However, the 2D layout of the chip limits the qubit connectivity and the low temperature requirement poses some engineering challenges (for details please refer to section 6, where challenges and bottlenecks are discussed).

Superconducting qubits are currently being used in a variety of research and development efforts for quantum computing, including in experimental systems that claim to have achieved quantum supremacy.

Some companies building quantum computers with superconducting qubits include IQM, IBM, Google, Rigetti, Alice and Bob, and Oxford Quantum Circuits.

2.2 Trapped Ions

Another possible realization of a qubit is the electronic state of an ion trapped in an electromagnetic trap. A saddle-like rotating potential keeps the ions in place while laser pulses perform gate operations and readout the measured states (via fluorescence).

Two-qubit gates are performed by coupling the (de)excitation of an ion to the vibrational modes (phonons) of the entire ion chain, followed by coupling the phonons to the (de)excitation of another ion, effectively performing a controlled-not gate. This approach allows to easily apply two-qubit gates on any pair of qubits.
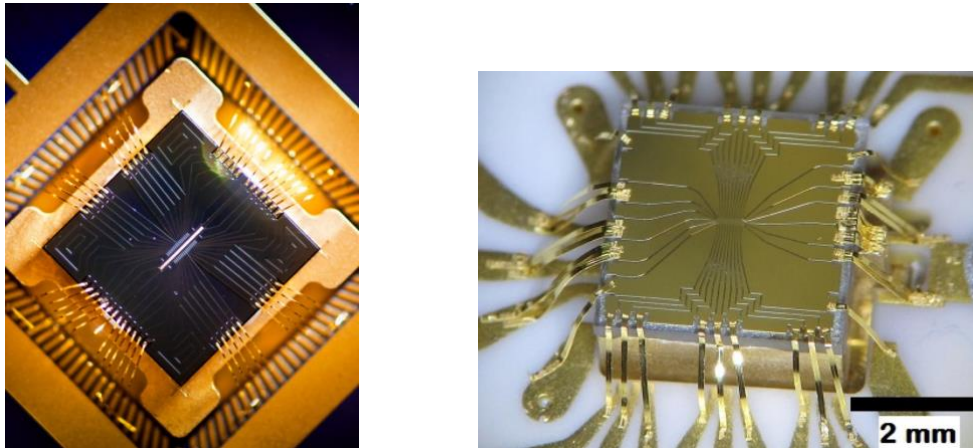
Figure 2: (Left) Surface trap fabricated by Sandia National Labs, supported by IARPA. This type of trap has been used to capture ions at JQI and Duke University, as well as other institutions. (Right) A planar rf ion trap from NIST designed for experiments with magnetically-driven quantum gates ([NIST23]).

QC based on trapped ions can achieve record 2Qubit gate fidelities. Scaling to larger Qubit numbers is currently investigated with surface chip traps (see Fig. 2). Material challenges and limitations of this approach with respect to scaling are discussed in section 6 (and also in [Leon21]).

"Trapped ion set-ups have been the first successful platform for the demonstration of quantum information processing (including Shor's algorithm for factoring numbers and quantum chemistry), with long qubit coherence times and high fidelities demonstrated for state preparation, single-, two- and multi-qubit gates, and state detection. All building blocks for initialization, manipulation and readout have been demonstrated at the fault-tolerant threshold." [QFS]

Some companies building quantum computers based on trapped ions are Quantinuum, IonQ and AQT.

2.3 Neutral Rydberg Atoms in Optical Lattices

Similar to trapped ions, a cold-atom quantum computer involves atoms suspended in vacuum. However, cold atoms are neutral and so can't be suspended in an electromagnetic trap. Instead, the technology holding the cold atoms in place are the so-called optical tweezers or optical lattices. These technologies rely on rapidly oscillating laser light holding the atoms in place due to the Stark effect.
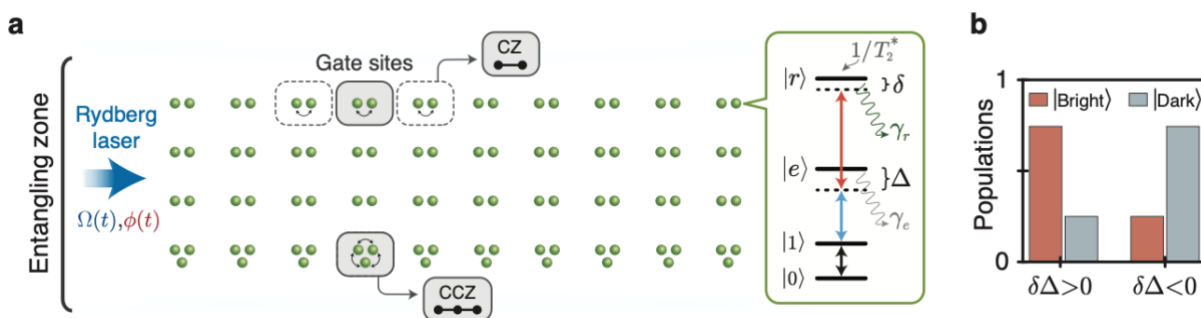

Figure 3: Parallel implementation of high-fidelity entangling gates on a neutral atom quantum computer. (a) Entangling gates are implemented by arranging atoms into designated gate sites where they interact via Rydberg

blockade interactions. (b) Numerical comparison of average bright and dark state populations during the Rydberg gate ([Evered23]).

Similarly, to trapped ions, the atoms are again manipulated using focused laser pulses. However, in the case of cold atoms, multi-qubit gates are executed taking advantage of a so-called Rydberg blockade. One atom is driven to excite from the ground state to a highly excited Rydberg state. Then a second nearby atom is driven by a similar laser pulse. If the first atom got excited, it is blockading the excitation of the second atom, effectively creating entanglement.

"Neutral atoms have been used successfully in optical lattices or tweezer arrays (with Rydberg atoms) for some of the largest scale quantum simulations to date, with promising applications also for quantum computing. Next to long coherence times and single atom addressability, they offer direct scalability towards 10^3-10^4 particle size systems. Today, they have already enabled some of the most complex and advanced quantum simulations with applications from material science, high-energy physics to statistical physics, and in many cases, already in computationally intractable regimes." [QFS]

Quite recently the MIT team around Vladan Vuletic (one of the QuEra founders) reported an important milestone, i.e. the realization of two-qubit entangling gates with 99.5% fidelity on up to 60 atoms in parallel, surpassing the surface code threshold for error correction (see Fig. 3.) [Evered23].

Companies using cold atoms are QuEra, Pasqal, Cold Quanta and planqc.

2.4 Photonics

Another medium for qubits can be photons. The state of a qubit can be encoded either in the polarization, position, or number of photons within an optical wire. There are several ways to do quantum computing with photons.

A well-understood non-universal protocol is so-called Gaussian boson sampling (GBS), which is described in detail later.

For universal photonic quantum computation, the most promising approach currently seems to be the one suggested in [Bourassa21]. This protocol first generates many self-error-correcting GKP states, using GBS-like devices. These states are entangled together into a cluster state and then measured in a measurement-based quantum computing protocol. Many such modules can be linked with optical fibers to increase the overall number of logical qubits to scale towards error correction, however this is still very far away.

Generally, photons don't tend to interact very much with air or each other. This means that qubits can be sent long distances and don't need very low temperatures or pure vacuum to operate. On the other hand, this makes entangling photons difficult. Many processes in photonic QC are non-deterministic, making scalability a potential issue.

"Integrated quantum photonics has enabled the generation, processing, and detection of quantum states of light in high component density, programmable devices, supporting multi-qubit operations.

With low decoherence properties, photonics provides routes toward Noisy Intermediate Scale Quantum (NISQ) era machines that outperform classical computers in solving industrially relevant problems. Manufacturing a fault tolerant universal quantum computer in photonics is now being pursued commercially. Single photon sources and photon-photon interactions, mediated through light-matter interaction, provide significant reductions in overheads in this compelling model." [QFS]

The main players attempting to build quantum computers based on photonics are Xanadu, Quandela, PsiQuantum and QuiX Quantum.

2.5   Solid State Qubits (Semiconductor Quantum Dots & Defect Centers in diamond)

Creating qubits with solid state spins involves manipulating the spin state of electrons, holes or nuclei within a solid state material. To create a qubit with solid state spins, a material with suitable spin properties is selected. The material is then prepared using techniques such as ion implantation or chemical vapor deposition to introduce defects or impurities into the material that can act as quantum bits. The qubits can also be defined lithographically using standard semiconductor techniques, such as those used for FinFET (see Fig. 4.), MOSFET devices, along with voltage gating. The qubits can then be controlled using microwave or voltage pulses.

Another approach is to use a type of defect in diamond called the nitrogen-vacancy (NV) center, which consists of a nitrogen atom replacing a carbon atom in the diamond lattice, with a nearby vacancy in the lattice. The NV center has a spin that can be manipulated using microwave and radio-frequency pulses, and can be used as the basis for a qubit.

"Semiconductor-based qubits make use of today's electronics technology. Employing nanofabrication techniques, quantum dots have been defined in which individual electrons can be confined. Also, isolated donors have been positioned in semiconductor substrates and used to trap individual electrons. In both cases, the spin of one or more electrons is considered the most promising qubit representation, since spin coherence is longer than the coherence of charge states or other degrees of freedom. These devices can be measured and controlled fully electrically, again much like transistors in today's digital electronics.[QFS]"

The companies working on spin qubits include Intel, Diraq, Quobly, Quantum Motion, Silicon Quantum Computing and Quantum Brilliance.
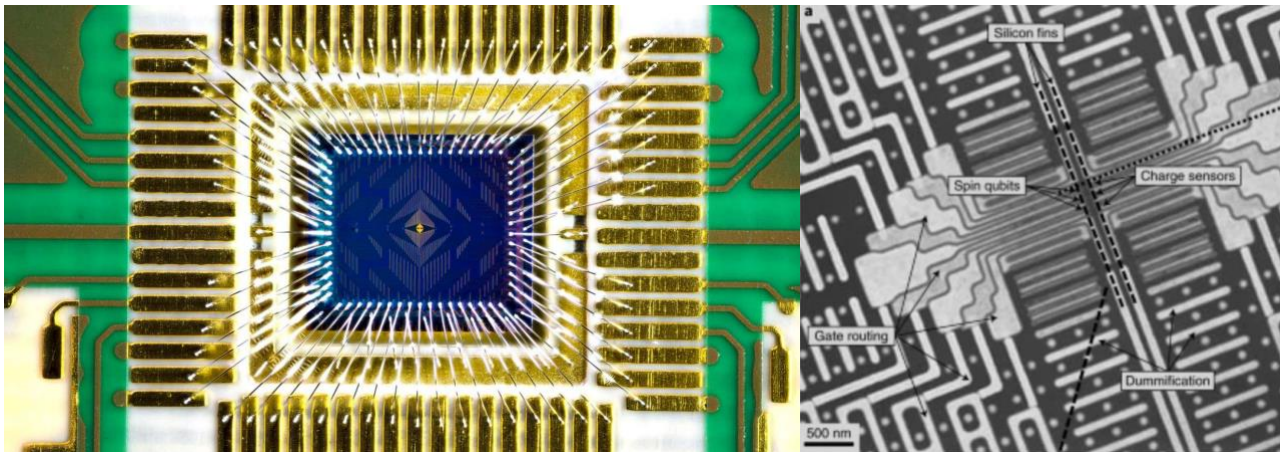
Figure 4: (Left) *Intel Tunnel Falls chip (12 qubits) in packaging [Intel23]* **(Right)** *Scanning transmission electron microscopy of a CMOS FinFET based spin qubit device [Zwerver22].*

2.6   Topologically protected qubits

"Topologically protected qubits are prominently developed in semiconductor nanowires hosting Majorana zero modes at their edges but are also being pursued in other platforms. While the existence of Majorana Fermions seems experimentally established, operating them and meeting all of DiVincenzo's criteria is a current frontier. It is believed that owing to their topological stability, once this is met, high performance can be reached with little overhead. Several other platforms for topologically protected qubits are being pursued, including Strontium, Ruthenate, Fractional Quantum Hall Systems, and Josephson Junction arrays. [QFS]"

The quantum team at Microsoft is developing a QC based on so-called "Majorana zero modes" (MZM). The quantum gates are applied by braiding the movement of these quasiparticles through time and space. The braiding makes topological qubits resilient to external noise, making potential future scaling relatively simple. However, at the moment the technology is very early, with no conclusive MZM demonstrations so far. However, there have been MZM simulations on other QC platforms [Mi22, Quantinuum23].)

2.7   Non-universal QC Technologies

There are several technologies based on the QC platforms mentioned above which don't satisfy DiVincenzo's 4th criterion (universal gate set), but which however hold the potential for useful quantum advantage in very specific tasks.

2.7.1   Quantum Annealing based on Superconducting Technologies

Superconducting qubits can be used for quantum annealing. In this adiabatic algorithm, the Hamiltonian of the system is slowly changed from a trivial case to the Hamiltonian describing a difficult optimization problem. If the process is slow enough, the qubits remain in the ground state of the Hamiltonian. Therefore, at the end of the quantum annealing process, the state of the qubits encodes the solution of to the optimization problem.

The main companies working on this form of quantum annealing are D-Wave and Qilimanjaro.

2.7.2 Quantum Simulations with Ultra-Cold Neutral Atoms

"Quantum simulation, a sub-discipline of quantum computation, can provide valuable insight into difficult quantum problems in physics or chemistry. Ultracold atoms in optical lattices represent an ideal platform for simulations of quantum many-body problems. Within this setting, quantum gas microscopes enable single atom observation and manipulation in large samples. Ultracold atom–based quantum simulators have already been used to probe quantum magnetism, to realize and detect topological quantum matter, and to study quantum systems with controlled long-range interactions. Experiments on many-body systems out of equilibrium have also provided results in regimes unavailable to the most advanced supercomputer" [Gross17].

2.7.3 Boson Sampling

As the name suggests, boson sampling refers to the protocol of sampling from a probability distribution generated by bosonic particles. Experimentally, the bosons are typically photons (or Gaussian states of photons). The bosons are generated in a collection of input wires, sent through an optical setup (called an interferometer) and eventually their location in a collection of output wires is measured, generating a sample.

A GBS device can not perform universal quantum computation, but its output is difficult to simulate, with several papers using it to claim quantum supremacy [Zhong20, Madsen22]. The interferometer can be programmed according to a specific mathematical graph, which causes the measurement results to correspond to subsets of the graph with relatively high edge density. This can be used to find dense subgraphs / cliques, which is an NP-hard problem with applications in many different fields (computer science, finance, sociology, logistics, etc.).

2.8 Hybrid Quantum Computing

Hybrid quantum computing refers to the setup in which part of the computation is done on a quantum computer and part on a classical computer (usually a high-performance computer). In principle this allows to off-load the classically-difficult part of the computation to the quantum computer while the classical computer does the part of the computation which it can do comparatively better.

Hybrid quantum computing is not a QC platform per se, as any of the above-mentioned platforms can be used in a hybrid QC solution. However, it is important to be aware of the specifics of hybrid QC and how it differs from standard simple QC.

Firstly, hybrid QC by definition includes distinct algorithms with a quantum part as well as a classical part. Presently the most commonly used hybrid algorithms include variational algorithms in which a quantum computer repeatedly runs a parametrized quantum circuit and a classical computer decides how to set those parameters for future runs. These fall broadly in two categories: optimization algorithms (QAOA, VQE) and machine learning (QNN).

Secondly, considerably different metrics matter for the efficiency of hybrid QC than for standard QC. Usually, high qubit number is not as important as for some standard algorithms (Grover's, Shor's). Instead, the parameters that matter are the fast execution of quantum gates (so that the classical computer does not need to wait for the quantum computer) and a low-latency, high-bit rate connection between the classical

and the quantum computer. For these reasons hybrid QC calculations tend to use superconducting qubits hosted physically on-site in an HPC center.

3   Technology Maturity Assessment

3.1   Metrics (Figures of Merit) for Evaluating Quantum Computing Hardware

There are many ways to evaluate quantum computers. The most simple approach is looking at the basic technical parameters of the QC, such as the number of qubits, the average gate fidelity, the average gate time or the connectivity of the qubits. However, a combination of these metrics is required for the quantum computer to be useful. To simplify the evaluation, various institutions and companies have introduced new composite metrics, such as the quantum volume, the Quantum Technology Readiness Level or the number of algorithmic qubits [IonQ22]. These try to reflect the impact of all the relevant parameters to evaluate the usefulness of the quantum computer in a single number. Here we first introduce all relevant basic technical quantum-metrics. For a mature and professional technology assessment we finally apply a high-level metric, i.e. Quantum Technology Readiness Level (QTRL) which was recently introduced by FZJ as a quantum counterpart to the NASA TRL-scheme.

3.1.1   Number of Qubits

Qubits are the basic units of information in QC. The number of available qubits is therefore a natural quantity to evaluate various QC technologies.

It is believed that a number of qubits ~50 is required to achieve the first meaningful quantum advantage. Many of the QC companies have already built QC with >50 qubits (or they are very close on their roadmaps). For reaching NISQ quantum advantage, the qubit number therefore isn't as important as the other metrics. However, for solving industrial-relevant problems, we often require many more qubits.

Furthermore, large number of qubits are necessary for reaching the fault-tolerant regime of quantum computation. In this regime, large number of (physical) qubits form an error-correcting code representing a much smaller number of logical qubits. Estimates for the number of physical qubits required for fault-tolerant quantum computing (FTQC) lie around a million.

3.1.2   Gate Fidelity / Error

The gate fidelity represents the accuracy of executing quantum gates on a quantum computer. In current technologies, the fidelities of 2-qubit gates are much lower than the fidelities of single qubit gates, making the 2-qubit gate fidelities the relevant bottleneck.

In the long term, quantum error correction allows one to increase the logical gate fidelity arbitrarily high at the cost of using many physical qubits to represent one logical qubit.

Sample data from 2021 comparing qubits based on 3 different platforms are plotted in fig. 5. It should be noted that these numbers are different from the system level fidelities available on actual QCs.
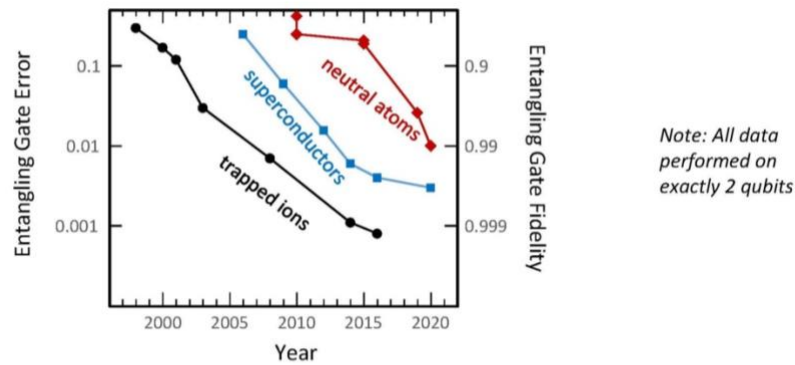
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Figure 5: SEQ Figure *Experimentally demonstrated two-qubit (entangling) gate fidelities [STH21]. Data from experiments prior to 2021. Note that system level two-qubit gate fidelities from leading vendors vary widely from the plot above.*

3.1.3   Qubit Connectivity

Many quantum algorithms require applying quantum gates between arbitrary pairs of qubits. Without high qubit connectivity, swap gates are required to bring the target qubits close to each other, increasing the depth of the circuit.

Trapped-ion QCs allow for 2-qubit gates between any pair of qubits, effectively having complete connectivity. Superconducting qubits and cold atoms are often arranged in a square grid, although various other topologies exist (such as the star topology by IQM or the heavy-hex topology by IBM). Those have advantages / disadvantages with respect to manufacturing and applicability for specific algorithms, but ultimately the 2D structure of the chip is a limitation.

3.1.4   Quantum Volume

A quantity called quantum volume has been defined and redefined several times in the past. Currently the most commonly used one is the one defined by IBM in [Cross19].

Based on the assumption that one executes a specific random circuit on the quantum computer (see figure 6) the quantum volume is then defined simply as:

$$\log V = \min(n, d)$$

Where n is the number of qubits and d is the depth of the circuit that we can run before the heavy output probability of the result drops below 2/3 from the noiseless value $(1 + \ln 2)/2$ (indicating that the output is too noisy).
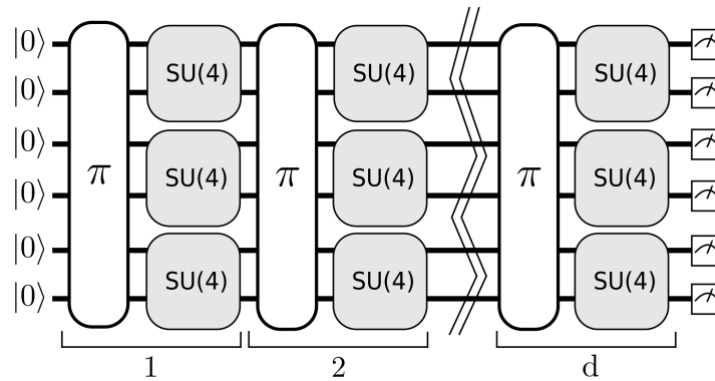
Figure 6: *The circuit used for calculating quantum volume. The π gates represent random permutations among the qubits, the SU(4) gates represent random 2-qubit gates. Figure from [Cross19]*

Quantum volume offers a compromise between qubit number, gate fidelity (high gate fidelity allows for larger values of d) and qubit connectivity (high connectivity makes the permutation gates easy to implement). Presently, the variable d is the bottleneck to reaching high quantum volume for most quantum architectures. This is due to too low gate fidelity or bad qubit connectivity (or both). Ion traps have all-to-all qubit connectivity and good gate fidelity, allowing them to reach world-record values of quantum volume.

3.1.5 Simplified Metrics

It should be emphasised that using just the standard metrics such as qubit count and gate fidelities can lead to misleading conclusions. In general, there were two metrics that significantly influenced our classifications and our view on when they could provide an advantage in applications. These are:

1. **Cycle time:** determines how long a single algorithm execution run will take on a particular platform. Different platforms have different time scales to perform gates, reset, perform state preparation, resulting in different total execution time. These numbers sometimes vary quite widely between platforms and is an important criterion when comparing QCs with classical systems.

2. **Number of qubits times the 2-qubit gate fidelity:** in order to perform algorithms in the near term, we need both a high number of qubits, which dictates the breadth of the circuit that we can implement, as well as a good gate fidelity, which determines the quality of execution. Different platforms have their advantages and disadvantages, which could skew their metrics one way or the other. However, a holistic view considering both these numbers provide a good metric to being able to provide quantum advantage.

3.1.6 Quantum Technology Readiness Level (QTRL)

Measuring respectively evaluating the performance of any quantum-computer based on the basic metrics introduced above is done best with the Quantum Technology Readiness Level (QTRL) [FZJ22], which is a heuristic metric on a scale of 1 to 9 that rates how far a given quantum technology has progressed on the path from the earliest ideas towards full-scale adoption in the society (see figure 7).
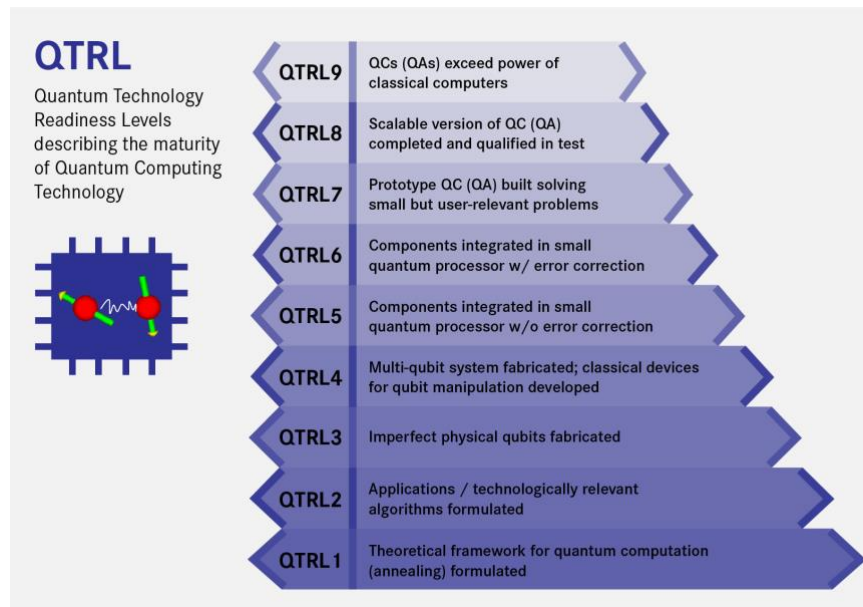
Figure 7: Quantum Technology Readiness Level (QTRL).

Definition of Quantum Technology Readiness Level (taken from [FZJ22])

« *A quantum computing technology is at QTRL1 when the theoretical framework for quantum computing (annealing) is formulated. Theoretical studies of the basic properties of the quantum computing (annealing) devices move towards applied research and development. The technology reaches QTRL2 once the basic device principles have been studied and applications or technologically relevant algorithms are formulated. QTRL2 quantum computing technology is speculative, as there are little to no experimental results supporting the theoretical studies.*

Fabricated imperfect physical qubits, the basic building blocks of quantum computing devices, are at QTRL3. Laboratory studies aim to validate theoretical predictions of qubit properties. Theoretical and laboratory studies are required to determine whether these basic elements of the quantum computing technology are ready to proceed further through the development process.

During QTRL4, multi-qubit systems are fabricated and classical devices for qubit manipulation are developed. Both components of the quantum computing technology are tested with one another. QTRL5 quantum computing technology comprises components integrated in a small quantum processor without error correction. Quantum computing devices labelled as QTRL5 must undergo rigorous testing including running of various algorithms for benchmarking. Components integrated in a small quantum processor with error correction are at QTRL6. Rigorous testing and running algorithms is repeated for the QTRL6 quantum computing technology.

QTRL7 quantum computing technology is a prototype quantum computer (annealer) solving small but user-relevant problems. The prototype is demonstrated in a user environment. A scalable version of a quantum computer (annealer) completed and qualified through test and demonstration is at QTRL8. Once quantum computers (annealers) exceed the computational power of classical computers for general (specific) problems the quantum computing technology can be labelled with QTRL9. »

3.2 Application of Metrics in this Assessment

Various QC metrics, in addition to the ones mentioned above were systematically studied for different platforms. These are detailed in the Excel file submitted along with this report. Although all the different metrics are not provided by the QC manufacturers, by studying these numbers from different vendors, we were able to fill in the gaps within specific platforms and make holistic decisions. Furthermore, QTRL classifies the platforms broadly, considering overall qubit numbers, error correction capability etc. However, gaining useful insight regarding the platforms using such a metric is difficult, as we will see in next section, that the major platforms are more or less at the same QTRL level. This however does not mean that the platforms are equally advanced. Instead, there are differences not captured by this broad generalization, which heavily influences how much value the platforms can provide in the coming years. Taking these differences into account, we can extrapolate the readiness level to the medium term (5-10 years), as detailed in the final table comparing different platforms suitable to the identified algorithms. These classifications required comparing various technical details of these platforms (detailed in the Excel file).

Platform	Current QTRL	Comments on evaluating
Superconducting qubits	5-6	Many companies have built small superconducting computers and papers have been published solving toy versions of user-relevant problems on them, including quantum error correction. Quantum error correction experiments on small QPUs performed successfully (see e.g. [Acharya23]).
Superconducting qubits (quantum annealing)	5	Many experiments were done on D-Wave quantum annealers, including error correction. Primitive error correction techniques available out of the box (DWave). However, QTRL6 not reached yet.
Trapped ions	5-6	Many companies have built small trapped-ion quantum computers and papers have been published solving toy versions of user-relevant problems. Quantinuum has demonstrated CNOT gates between logical qubits and has published papers solving toy-problems with error detection. Real-time quantum error correction experiments on small QPUs performed successfully (see e.g. [Ryan-Anderson22]).
Cold Rydberg atoms	5	Toy problems [Evered23] have been solved there. However, QTRL6 not reached yet.
Photonic	5	Gaussian Boson sampling performed by industrial and academic players. Universal photonic QC is at QTRL3.
Solid State Qubits (Semiconductor and NV-centers)	5-6	Small toy problems have been solved, including demonstration of QEC. Quantum Error Correction on small QPUs performed successfully (see e.g. [Takeda22]).
Topological qubits	2	Microsoft is focused on developing topological qubits.

4   Industrial Roadmap Assessment (mostly taken from [Koennecke22])

The roadmap for completion of new prototypes promised by the ecosystem is extensive, with at least 20 new devices trumpeted by the respective key players between now and 2030 (see fig. 8).
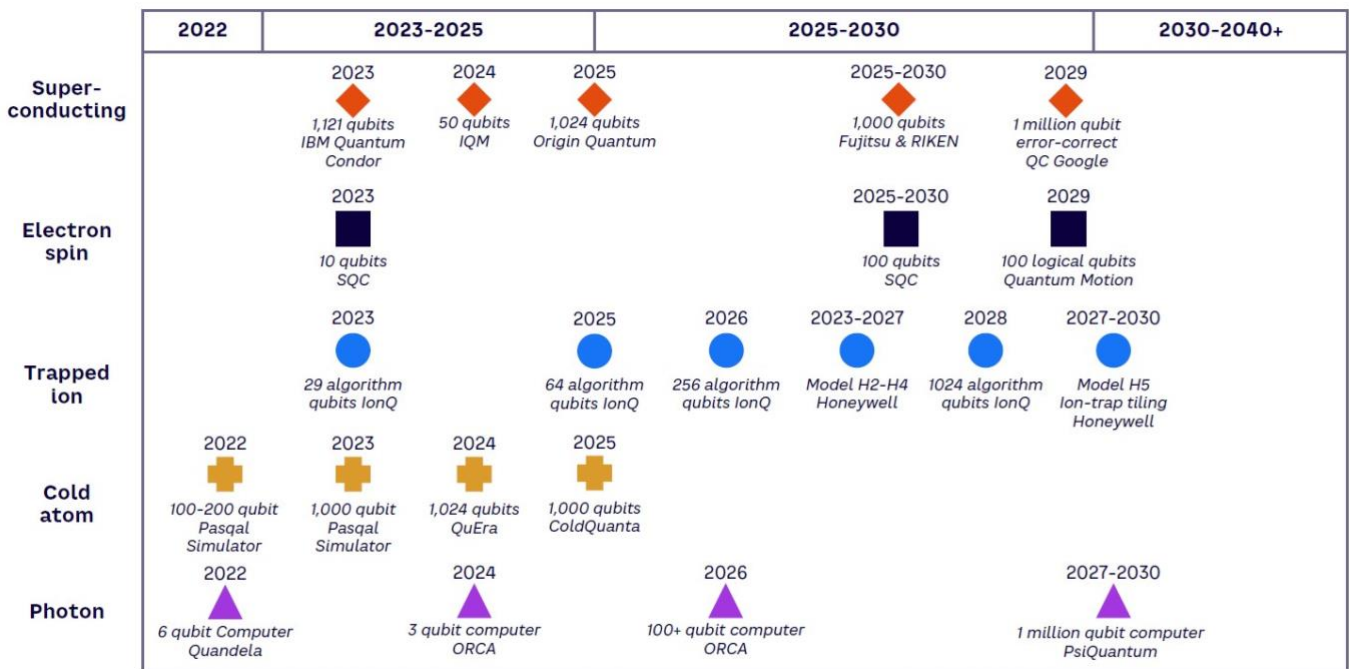
Source: Arthur D. Little, Olivier Ezratty

Figure 8: *Quantum computing prototypes on vendor roadmaps [Koennecke22].*

« *As shown in Figure 8 a 1,000+ qubit machine such as the IBM Quantum Condor could be available as early as 2023. Looking further ahead, a 1 million qubit machine could be available before 2030. However, given the remaining technical challenges and uncertainties, this should best be viewed as an optimistic projection. A more conservative assumption would be that the key milestone of achieving a fault-tolerant large-scale quantum computer might occur in the range 2030-2040.* » [Koennecke22]

« *Currently, it might be reasonably concluded that the Superconducting technology is the most likely candidate to become commercially available for practical use in the next decade. But the technology development path at this limited level of maturity, and with this level of complexity, is rarely linear. If one of the other competing technologies achieves a breakthrough, it is possible that it could leapfrog the others.* »[Koennecke22]

In addition to the above survey from Artur D. Little [Koennecke22], *Ian Hellström* has collected a "*summary of quantum computer roadmaps*" [Hellstroem23a] for various qubit modalities and vendors, including references to official sources. Qubit modalities include superconductors, trapped ions, neutral atoms, quantum dots, photonics, spin (i.e. nitrogen vacancy centres in diamond), NMR, and quantum

annealers. For each quantum computer generation, the number of physical qubits (see fig. 9), and, where available, quantum volume, logical qubits, relaxation times, and gate fidelity statistics are listed.
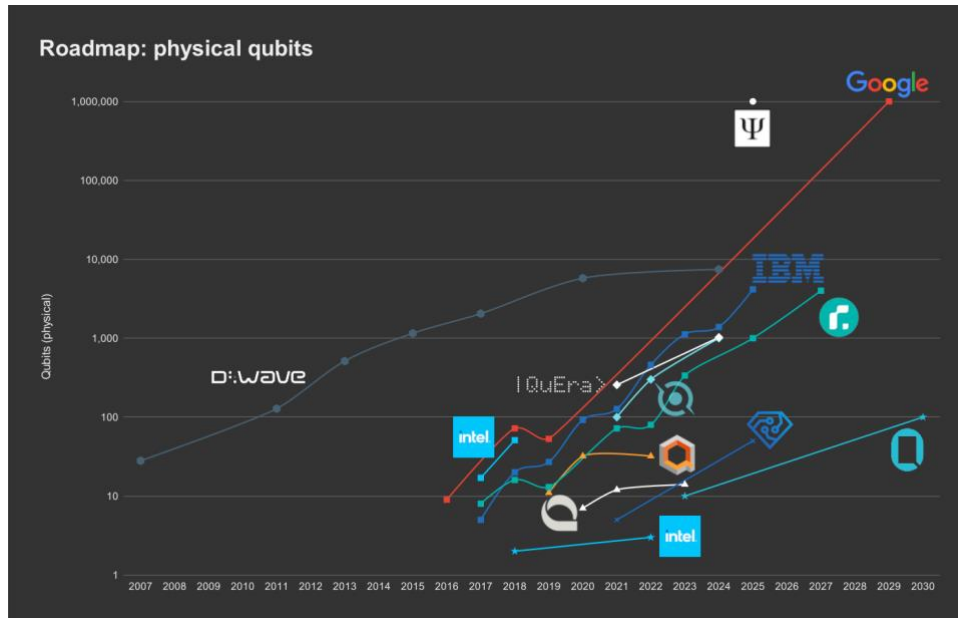

Figure 9*: Quantum computing roadmaps for the number of physical qubits (taken from [Hellstroem23b]).*

Evaluating the published roadmaps is difficult for several reasons. Some HW vendors provide elaborate roadmaps while others only give very vague indications. Furthermore it is often difficult to distinguish marketing from science-based prognosis.

For those reasons we based our analysis mostly on physical parameters and metrics, which mostly depend on the platforms and not so much on the HW manufacturer.

Nevertheless, QC development already has several years of history, so we can look at those datapoints and attempt to extrapolate or at least provide some observations that can guide our view of the future.

1) Historically, quantum annealers based on superconducting qubits (produced by D-Wave) have always been larger than their contemporary gate-based quantum computers, due to their choice of less-complex architecture of flux-based qubits. They still remain one of the best options for solving combinatorial optimization problems, but recently gate-based QCs have been catching up.

2) The most comprehensible roadmap is the one provided by IBM. It contains a lot of details, but as of July 2023 it only provides specific milestones up to 2025. However, recently they provided an updated milestone of a 100,000 qubit quantum-centric supercomputer by 2033, comprising of four 25,000 qubit clusters. IBM has so far achieved the goals set out in their past roadmaps, giving their predictions credibility.

3) Some companies provide roadmaps with significantly fewer data points or weaker evidence of achieving milestones in the past (such as photonic QC companies).

4) Google was one of the first to claim achieving quantum supremacy, however it is difficult to reliably extrapolate from that to predict when they will achieve 1,000,000 qubits.

5) Most of the roadmaps focus on qubit numbers instead of other metrics, such as fidelity (arguably more important). The exception is IBM with their 100x100 challenge and IonQ which publishes their roadmap with algorithmic qubits instead of physical qubits [IonQ22].

5 Risk/Opportunity Assessment

Technology	Opportunities	Challenges / Risks / Bottle Necks
Superconducting	• Fast gate and cycle times. • Good device metrics (gate fidelity etc.) • Compatibility with existing fabrication techniques • Long range connectivity possible (IQM co-design platform) • Large qubit arrays demonstrated (few 100)	• Short coherence times (transmon qubits) • Low connectivity (mainstream architecture) • Large form-factor qubits • Wiring bottleneck for scaling to QPUs with > 200 Qubits [Krinner19, Acharya22]
Trapped Ions	• Long coherence times • High gate fidelities • Easier connection between QCs, and to networks via optical link (might require optical cavity)	• Slow gate time (resulting in longer cycle time) • Number of ions in a single trap limited by frequency crowding. • More difficult to scale; fewer qubits demonstrated compared to other platforms. • Scaling to > 100 qubits with planar ion traps hard due to fluctuating EM fields causing decoherence [Leon21] • Initialization: Long ion loading time • laser cooling needed.
Photonics	• Possibility of photonic chip based on Si, SiN (PsiQuantum) • Easier to connect to quantum network via optical link. • Modular architecture	• Significant photon loss (66%) restricting to specific compute architectures. • Heralding needed on most platforms (probabilistic source). • Probabilistic gates (post selection) • Photon detectors require cryogenic temperatures (2-10K)
Solid state spins (Silicon based, and NV-centers)	• CMOS fabrication compatibility • Large T1 times. • Scalable architecture with nano-scale qubits • On-chip integrated control electronics	• Fabrication on advanced nodes needed. • Short-range connectivity • Short T2* coherence times (semiconductor) • Cryogenic temperatures needed (though 4K operation demonstrated)
Cold Neutral Rydberg Atoms	• Long coherence times • Large qubit arrays demonstrated (few 100s) • High qubit connectivity and fidelity • Connection to quantum networks via optical links possible.	• Long gate times (for gate-based architectures) • Long cycle times • Significant initialization error of (60%) requiring post-processing to fill missing traps (see [Endres16]). • Trap lifetime (laser cooling needed) • Spontaneous avalanche dephasing in large Rydberg ensembles (see [Boulier17])
Topological	• Theoretically highly stable and protected from errors.	• Not demonstrated so far. Current demonstrations of Majorana Zero Modes have been challenged in academia.

The leading platforms are more or less tied when comparing various device metrics generally considered for benchmarking. However, considering risks and future timelines, a different picture starts to emerge which allows one to make a fair comparison between the platforms.

The technology with the lowest QTRL is the topological qubits based on Majorana Zero Modes, followed by Microsoft and Nokia Bell Labs. Although considered stable and noise-protected from a theoretical perspective, in practice, there has been no academic consensus of whether these particles have been demonstrated in devices.

Platform based on photonic qubits has been pursued by companies such as PsiQuantum, Xanadu, Quandela, NuQuantum etc. Although there is the promise of chip-level integration based on silicon photonics (PsiQuantum), and with Gaussian Boson sampling experiment performed by Xanadu and USTC, the limiting factor here is the very significant photon loss of around 60% in general. This is in-addition to the heralding needed in case of non-deterministic photon sources. These non-deterministic sources and gates restrict the platforms to certain architectures (Xanadu: measurement based; PsiQuantum: fusion based), without which these errors would add-up exponentially. Even with these architectures, the path to computation advantage is not straightforward.

Cold Neutral Rydberg Atoms (Pasqal, QuEra, Cold Quanta, planqc, Atom Computers etc.), is a platform that has shown good progress in number of qubits (Pasqal: 361 qubits). Although initially operated as a quantum simulator, digital operation has been demonstrated on this platform using hyperfine interactions. Although with very good coherence times, this platform could be limited by the very slow cycle times. Solving problems which require a large number of shots would take significantly long. The problem of non deterministic loading of trapping sites of arrays with single atoms can be overcome with the help of spatial light modulators resulting in the assembly of defect-free cold atom arrays [Endres16].   Quite recently the MIT team around Vladan Vuletic (one of the QuEra founders) reported an important milestone, i.e. the realization of two-qubit entangling gates with 99.5% fidelity on up to 60 atoms in parallel, surpassing the surface code threshold for error correction [Evered23]. By enabling high-fidelity operation in a scalable, highly-connected system, these advances lay the groundwork for large-scale implementation of quantum-algorithms, error-corrected circuits, and digital simulations. Nevertheless, the short lifetime of Rydberg states (a few 10 micro seconds) and the overhead to assemble large (> 100) defect free arrays of trapped atoms show road blocks to scale this approach beyond several 100 qubit QPU's.

Trapped-ion based QCs (Quantinuum, IonQ, Universal Quantum etc.) are a platform that has shown significant results both in terms of benchmarks, fidelities and coherence times. These systems have been demonstrated with only a few 10 of qubits so far due to frequency crowding issues in a single trap. And although other architectures (Quantinuum's QCCD) have been proposed to overcome these issues, the system still has long cycle times due to slow gates and measurement times, limiting its utility in applications needing long circuits with large number of shots. There are significant engineering challenges that have to be overcome to scale this platform to larger qubit sizes (>100) with integrated planar ion traps (see e.g. [Leon21]), preserving qubit coherence. .

CMOS based spin-qubit platforms (Intel, IBM, Diraq, Quantum Motion, Quobly etc.) are a new entrant to the quantum computing field, having demonstrated performance above error threshold only in the last couple of years. These are based on scalable, nanometer sized qubits built on standard CMOS technology,

which has decades of development behind it. This would make it a good platform for fault-tolerant QC, provided it can overcome significant challenges ahead of it, namely long readout times (without sacrificing fidelity and scalability), low T2* coherence time, and signal routing at the nanometer scale (see e.g. [Leon21]). The largest QPUs demonstrated so far only has 12 qubits, from Intel.

Although some of the highest-fidelity single-qubit and two-qubit gates have been demonstrated with **NV centres in diamond** (99.9952% and 99.2%, respectively), efforts to scale in this platform are relatively immature as there are significant material problems to be solved (see [Leon21]).

The **superconducting qubit based technology** has been pursued for decades now, with significant years on the current mainstream transmon qubit alone. This has ensured that this platform has good metrics on almost all counts: qubit number, gate times, cycle times, gate fidelity and measurement fidelity. Although the coherence times are lower than some other platforms, the faster gate times ensure that there is no loss of circuit depth, and significant research focused on the materials side to improve these numbers. With the ability to interconnect qubits over a long range with resonators and a simple fabrication technique, this platform has a very clear path to scalability, as evident in the detailed roadmaps of several leading manufacturers like IBM, Google, and IQM. This would put this platform at the forefront of scalable technologies in the NISQ era. Moreover, cycle times are an important metric, which ensures that classically intractable problems can be solved in a reasonable time on quantum computers. This platform has one of the fastest cycle times, ensuring faster computation of application problems. Nevertheless, also this platform has its technological bottlenecks like the « wiring » problem [Krinner19]). Efforts to overcome this problem by multiplexing (see [Acharya22]) and using SFQ/AQFP-based cryogenic digital controllers [Takahasi22] are currently being undertaken, placing the superconducting technology clearly as the leading and most mature current quantum computing technology, securing its winning margin for the next decade.

6 Summary and Outlook for QC4EO Applications

Platform	Target UC	Current QTRL	Expected QTRL in 5-10 years	Vendors	Major technological challenges/bottlenecks to overcome	Potential risks	Integrated roadmap synthesis
Superconducting	UC1-QNN, UC2, UC3, UC4	5-6	8-9	IQM, IBM, Google, Rigetti, Amazon, Alice and Bob, Quantum Cicuits Inc., Oxford Quantum Circuits, Atlantic Quantum, Seeqc	Wiring problem when scaling to larger QPUs (> 200 qubits) requiring advances in wiring and/or cryogenic control chips; High-fidelity interconnects needed to connect different QPUs.	Cost to scale up without progress in cryogenic control and readout.	IBM has a detailed roadmap with some limited scaling by linking NISQ chips together. Google has a roadmap to 1M physical qubits (with QEC), emphasizing connectivity and making components smaller.
Ion Traps	UC1-QNN, UC2, UC3	5-6	8	Quantinuum, IonQ, AQT	Scaling up 2D traps while maintaining coherence of ions.	The long cycle time of operations could limit the potential applications that can be run on this platform.	Quantinuum is planning to use integrated optics to control the ions in the trap to allow for greater scalability. Also 2D traps
Cold Neutral Rydberg Atoms	UC2	5	7-8	Pasqal, Cold Quanta, QuEra, planqc, Atom Computing	Scaling up qubit lattices beyond a few thousand qubits while simultaneously improving trap filling and fidelity of operations.	Being unable to scale up beyond a few thousand qubits with good device metrics.	Currently scaling to ~1000 qubits is straightforward, gate fidelities the main bottleneck. Past thousands of gates, switch

							needed from optical tweezers to optical lattices, with a lot of potential problems.
Photonics	UC1-QAOA	5	8	PsiQuantum, Xanadu	Photon loss per gate/circuit.	Significant photon loss of 33% (seen in current architectures) will limit scaling.	Xanadu has a theoretical blueprint for scalable MBQC, but a lot of experimental progress is necessary. GBS currently possible, but not universally useful.
Solid State Qubits (Silicon and NV-center)	UC1-QAOA	6	8-9	Intel, Diraq, Quobly, Quantum Motion, IBM	Device variability and signal routing on large-scale QPUs and high fidelity readouts in short duration.	Various components needed for scaling up have been demonstrated only in small scale experiments. There could be delay/challenges to successfully integrate these peripheral components to the QPU to enable scaling up to large QPUs.	Solid state qubits are currently lagging behind on qubit numbers and/or fidelity. Idea is to take advantage of small size + fabricating technology to scale up to Ms and Bs of qubits in 10-20 years time.
Topological Qubits		2	3-4	Microsoft, Nokia Bell Labs	??	Unambiguous demonstration of topological qubits required.	Microsoft doesn't believe in NISQ. The path to scaling is topological

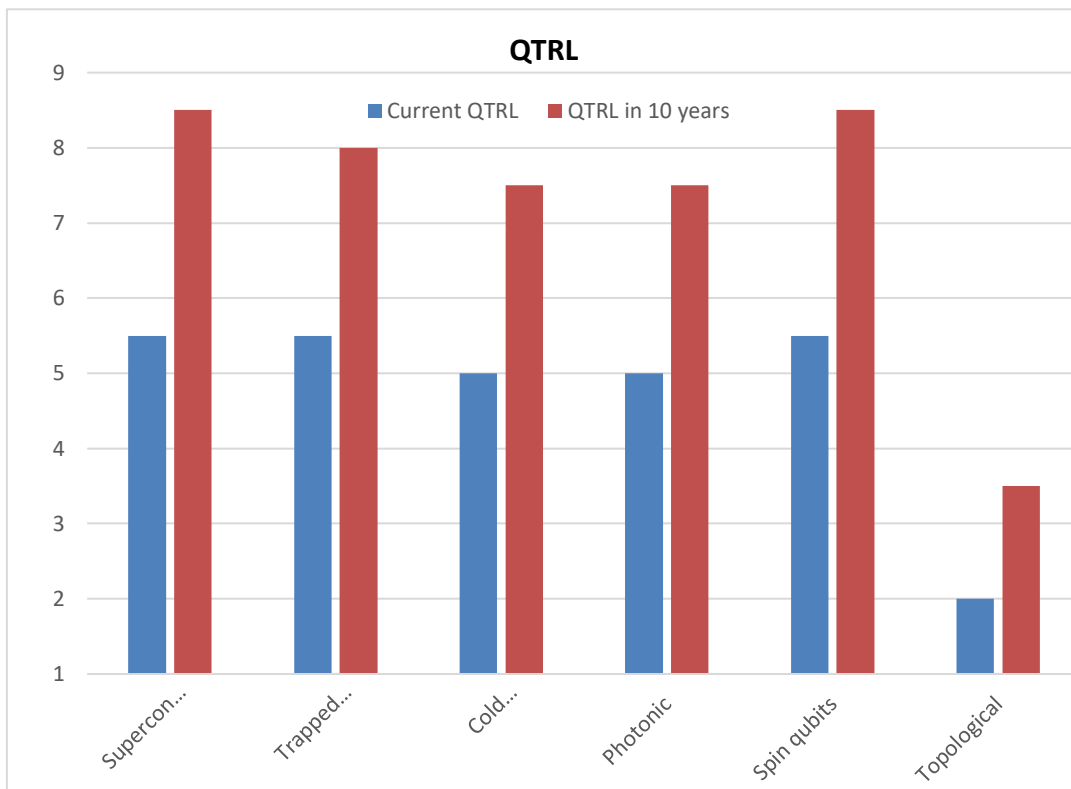|						qubit. So far they don't even have 1 qubit, but even if they make it, building a QC will be hard.

Figure 10 *: Measured QTRL of different hardware platforms 2023 (blue) and in 10 years (red).*

In the WP2 document, 4 use cases for quantum computers were analysed from a machine-sizing perspective (see table below). In this section we briefly comment on the suitability of various QC platforms for the use cases. For a more detailed analysis, please refer to the outcome of WP4.

It is important to distinguish between NISQ use cases and FTQC use cases, i.e. those that can be solved on noisy, intermediate-scale quantum computers and those that require larger or error-corrected machines. This can inform decisions about when any quantum advantage can be expected and which QC platform to target.

The first approach to UC1 transforms the mission planning problem into QUBO instance. QUBO problems can be solved by quantum annealing or its gate-based alternative, QAOA. Both of these are generally considered to be NISQ algorithms. However, in UC1, the number of variables and constraints leads to a QUBO formulation with a huge number of variables ($N_{var} \sim 10^6 - 10^9$). This is beyond the reach of any

NISQ quantum computer or annealer. Solving this problem with this method will therefore require truly scalable (and presumably error-corrected) quantum computers. Historically, quantum annealers have always offered more qubits than their contemporary gate-based quantum computers, but it is difficult to say whether this trend will persist for the next 15-20 years when such large qubit numbers can be expected. This use-case might therefore be most well suited for QC platform that scales the best in the long term (solid state qubits / photonics).

The second approach to UC1 uses a hybrid classical-quantum neural network. In this case, the quantum circuit uses a relatively modest number of qubits and circuit depth. Some of the proposed circuits are already in reach of present-day quantum computers. The number of qubits is likely not a bottleneck, but care should be taken that that chosen hardware has low enough error rate to faithfully execute the whole circuit. Superconducting qubits and trapped ions have high enough qubit numbers and low enough error rates to run the proposed circuits. If training of the neural network is expected to take a long time, then superconducting qubits give the advantage of fast circuit execution and interaction with the classical computer. As the quantum circuit requires only circular application of CNOT gates, limiting qubit connectivity is not a problem.

UC2 again contains two different quantum algorithms to consider. As before, the key point extraction problem can be reduced to a QUBO instance. As noted in WP2, analysing images of 3099x2329 pixels requires millions of qubits and therefore a fully scalable (error-corrected) quantum computer. Fortunately, the whole problem can be divided into small sub-problems, which can be solved individually. Finding the key points of a small image with just tens/hundreds of pixels will require correspondingly many qubits, which is within the reach of some of present-day quantum computers / annealers. However, the all-to-all connectivity of the QUBO will inflate the required circuit depth for platforms with lower qubit connectivity (superconducting-qubit computers / annealers). The platforms of choice will then be ion traps if they manage to scale their computers up beyond low tens of qubits or SC qubits if they manage to increase the gate fidelity to support the required circuit depth. The required HW requirement lie in the NISQ era, although still roughly 5 years away.

The second algorithm considered in UC2 is a circuit for calculating the quantum kernel function. The circuit shown acts on 4 qubits with a depth of 52, something doable on present-day quantum computers on most platforms. One can design kernel functions on more qubits, with quadratically growing circuit depth. Together with the fact that the suggested kernel circuit requires all-to-all connectivity. Ion traps and neutral atoms have high connectivity natively, whereas for superconducting qubits, the problem needs to be addressed with extra swap gates or by co-designing the QPU to support the required connections. Such approach is possible if the quantum circuit is known beforehand, which is the case here.

The approach described in UC3 is again quantum kernel calculation. Generally, these algorithms can be expected to run on near-term devices, within the NISQ era. Depending on the details of the feature function, the resulting circuit may be suitable for ion trap devices with their high fidelities and all-to-all connectivity, or superconducting qubits with many more qubits, high fidelity, but worse connectivity.

The algorithm outlined in UC4 is Quantum Fourier transform (QFT). The algorithm allows to process huge amount of data on relatively few qubits (13-32 according to the WP2 report). Unfortunately the entire circuit is too deep for any NISQ computer to give accurate results, so quantum error correction is necessary. The low number of logical qubits needed suggests that the first platform to achieve scalable QEC (expected in 10-15 years) will be suitable for this application, but more theoretical progress is needed on uploading and downloading the classical data in/out of the circuit.

6.1   Conclusions and recommendations

A large part of the work in WP3 went into the collection and assessment of the different data from technologies (see attached EXCEL comparison table). Here we finally aim at providing an overall assessment taking into account on the one hand the EXCEL-table culminating in our QTRL-evaluation and on the other hand the vendor roadmap assessment. Of course, an overall comparative assessment remains subjective and speculative to a certain extend. If this would not have been the case, a clear winning technology would have already emerged on the QC market and all producers of quantum computing hardware would already now focus on this one and only technology.

In this investigative report we identified three leading technologies, which seem to have the highest maturity, i.e., superconducting qubits, trapped ions, and cold atoms. For these three technologies we consider the following five figures of merits (for details see also chapter 3.1 on metrics) as essential for describing and comparing the performance of actual quantum computing hardware (see Fig. 11):

- connectivity of qubits
- scalability of the qubits
- ease of executing quantum gates (gate-based model)
- gate fidelity
- speed of execution (circuit layer operations per second, CLOPS)

For the mentioned three main available technologies, superconducting qubits, trapped ions, and cold atoms, we can summarize the assessment of this report in the following single plot.
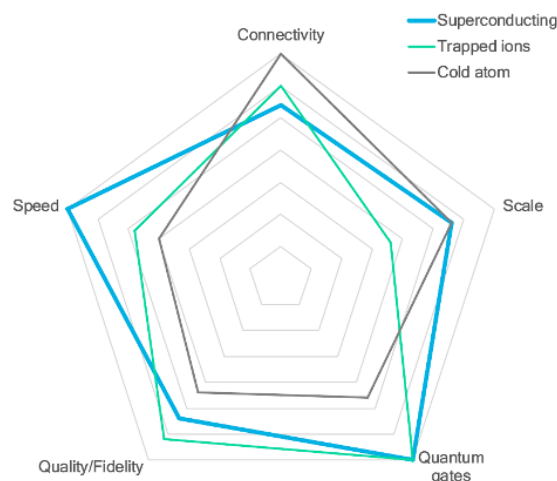

Figure 11: *Comparison of different leading quantum computing technologies.*

Whereas cold atoms are good on connectivity and scalability, they have some drawbacks on speed and fidelity in gate-based operations. Trapped ions are strong with respect to gate fidelity but face major drawbacks on speed and scalability. Finally, superconducting technology allows extremely fast quantum gate operations, shows good scalability, is excellent on quantum gate performance, and has sufficient fidelities for the machines to work in the short time scales required for executing quantum circuits.

In order to assess what this implies for commercial and scientific applications it is helpful to distinguish two-time scales in bringing the technology to the market:

- Near term (3-5 years): noisy qubits, small number of qubits, up to 1000 qubits (NISQ)
- Long term (10+ years): fault tolerant (error corrected) qubits, large number, up to 1 Mio qubits (FTQC)

For the NISQ era we need sufficient quality of qubits, but especially short gate times, as calculations are performed using many iterations of the quantum algorithm (to correct for errors). Thus, we conclude: that superconducting technology is superior, as trapped ions and cold atoms are a factor 1000 slower.

For FTQC we need sufficient quality of qubits, but especially scalability, and working error correction schemes. Superconducting technology is superior, as, e.g., trapped ions have prototypes for maximum 50 coupled qubits. Scaling beyond few 100 is at the moment unclear and faces some major technological drawbacks (see also risk assessment in chapter 5). Cold atoms are focussing mostly on simulations, and scaling to thousands of qubits is a huge challenge (for details see chapter 5).

Superconducting technology seems to be in the sweet spot of qubit stability, speed of calculation, and execution of the gate-based model, with sufficient fidelities. Together with the proven industrial manufacturability of the technology, we thus conclude that superconducting technology seems to be the only viable candidate for commercial and scientific applications of quantum computing that covers both near term (NISQ) and long term (FTQC).

On the vendor side we see a major player from north America, which is IBM, and a major player from Europe, which is IQM. Google does not offer quantum computers to the market, for the time being.

Amongst the two players IBM and IQM we acknowledge that IBM is longer in the field of quantum computing, but IQM has been picking up speed and has closed the gap to its' competitor. IQM's philosophy has been to focus on tunable couplers and tunable qubits, which allows to gain advantage in the field of fidelities.

High qubit numbers without sufficient fidelities is not useful, which may be the reason for IBM recently switching its' qubit architecture to tunable couplers. IBM so far on their technology roadmap has been concentrating only on scaling to high qubit numbers but did not realize that this approach will not allow sufficiently high gate fidelities. Through this switch in technology choice, we consider IBM and IQM to be roughly on the same pitch of their capabilities. IBM has focussed on the 100 x 100 challenge, i.e., executing 100 gate steps with 100 entangled qubits. Just as IBM, we see IQM being able to fulfil the 100 x 100 challenge in the next 1 or 2 years, as soon as IQM's 150 qubit machine is available (54 qubits are being tested and installed currently by IQM in the VTT computing facilities).

Two final remarks on near term and long-term comparison of IQM and IBM:

- NISQ: IQM is best in class, as IBM is a factor of 10 slower on gate times.
- FTQC: IQM is promising, as it is working on efficient co-design chips for error correction (factor 10 less qubits required).

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A.2 Identified Use Cases from WP2 midterm report

Table 1: Identified use cases of quantum computers using different types of quantum algorithms (this table is taken from the WP2 midterm report of QC4EO).

Use case	Quantum algorithms	Quantum instance
UC1 – Mission Planning for EO Acquisitions	•Quantum annealing •QAOA •Quantum NN	•Full quantum (QUBO problem on a quantum annealer) •Full quantum on a NISQ device •Hybrid (QNN as policy model within a RL framework)
UC2 - Multiple-view Geometry on Optical Images	•quantum k-medoids •quantum kernel densityclustering	•Hybrid: full quantum (QUBO problem + quantum kernel) for the quantum keypoint-extraction process then classical algorithms for image transformation tasks
UC3 – Optical Satellite Data Analysis	•quantum Kernel Estimation	•Hybrid: use of QC to calculate the Gram matrix that is then used in conjunction with some kernel-based classical ML algorithms
UC4 –SAR Raw Data Processing	•QFT	•Full quantum: Quantum range doppler algorithm

Table 2: Use-case related determination of the machine sizing (qubits, KPI) for different target platforms (taken from WP2 report).

Use case	Quantum algorithms	# qubits	KPI	Target platforms
UC1 – Mission Planning for EO Acquisitions	•QA •QAOA •QNN •*Tensor Network*	•Binaries in the cost function (including slack) and connectivity of the problemscale linearly with the system size (better with preprocessing) •Size of the input in QNN reducedwith a classical NN	•Physical qubits grow polynomially with pre-processing (D-Wave Advantage) •Number of gates per layer is polynomial in #qubits; layers scale log in #qubits •All characteristics of the circuit scale linearly in #qubits	•Quantum annealers •Quantum simulators: • superconducting •trapped ions

UC2 - Multiple-view Geometry on Optical Images	•Q k-medoids •Q-kernel density clustering	•Smaller subimage: 4 keypoints on 8x8 pixels down to 64 binaries •Kernel matrix 4 qubits circuit	•QUBO •All the characteristics of the circuit (#2-qubit gates, depth) are quadratic in the #qubits	• Quantum annealers • Trapped neutral atoms • Trapped ions
UC3 – Optical Satellite Data Analysis	•Q-Kernel Estimation	•Depends on the dimensionality of feature vector	•Depends on the feature maps	•superconducting
UC4 – SAR Raw Data Processing	•QFT	•Related to raw signal dimension •Amplitude encoding scales log, #qubits in [13,32]	•Circuit depth is expected to be a bottleneck, still under investigation	•superconducting •Trapped ions

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